

Figure 1

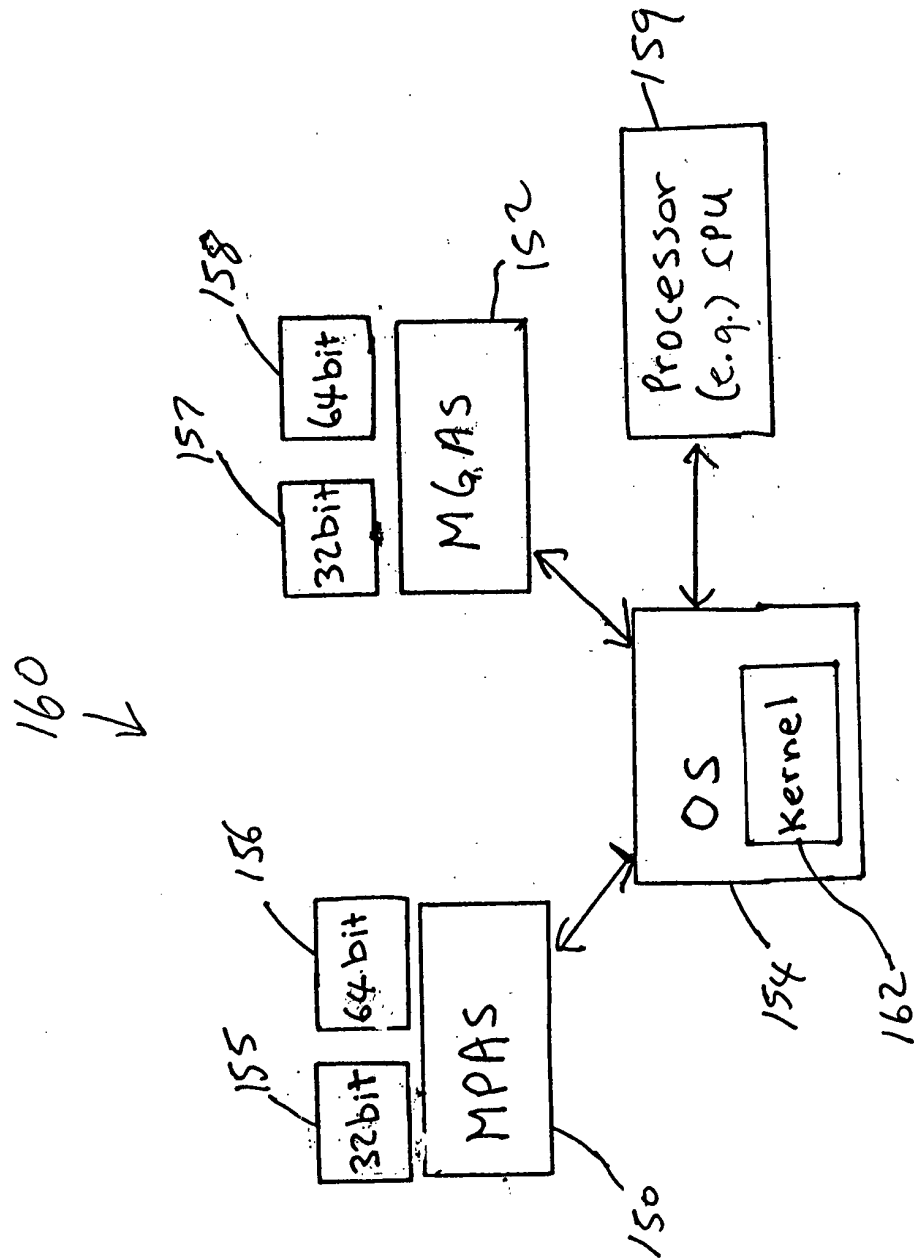
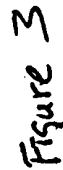


Figure 2



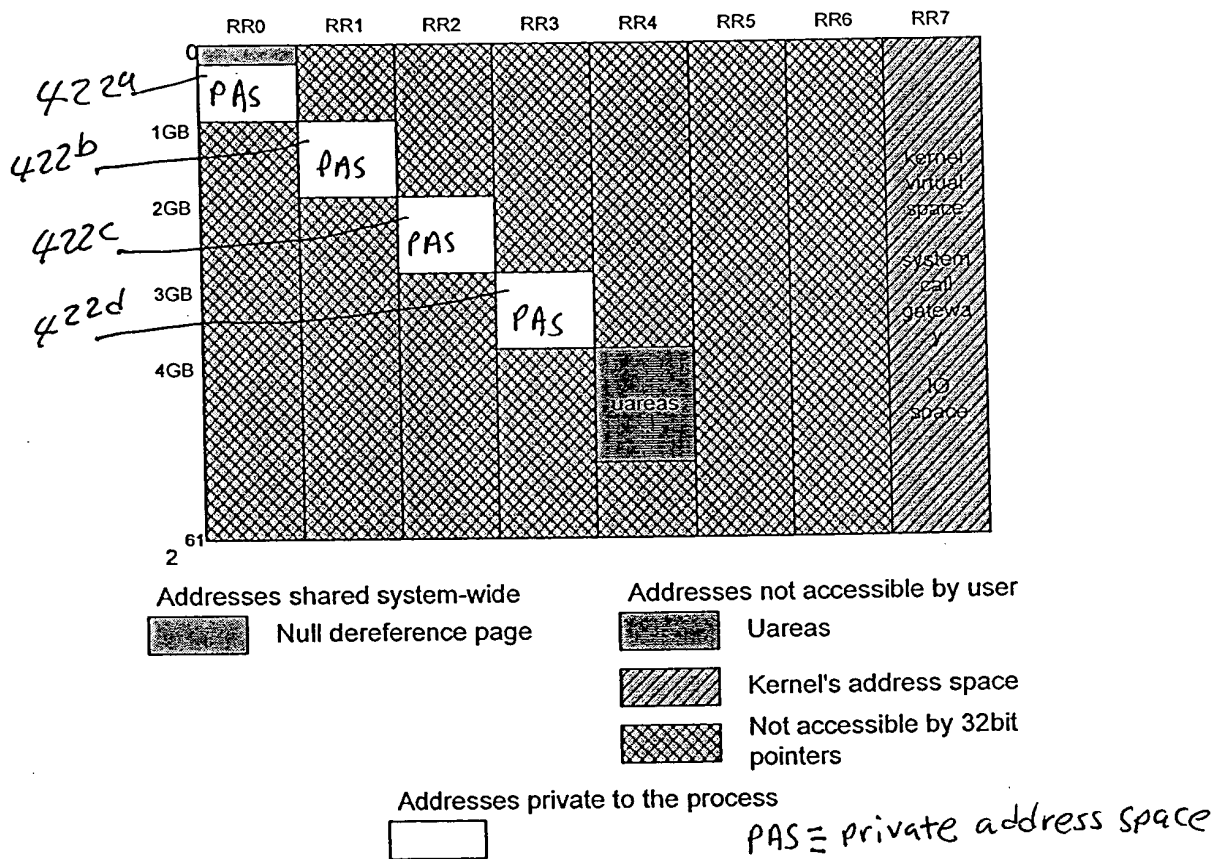


Figure 4A 32bit MPAS Address Space Layout (ASL) in segmented representation

METHODS AND APPARATUS FOR A DUAL ADDRESS
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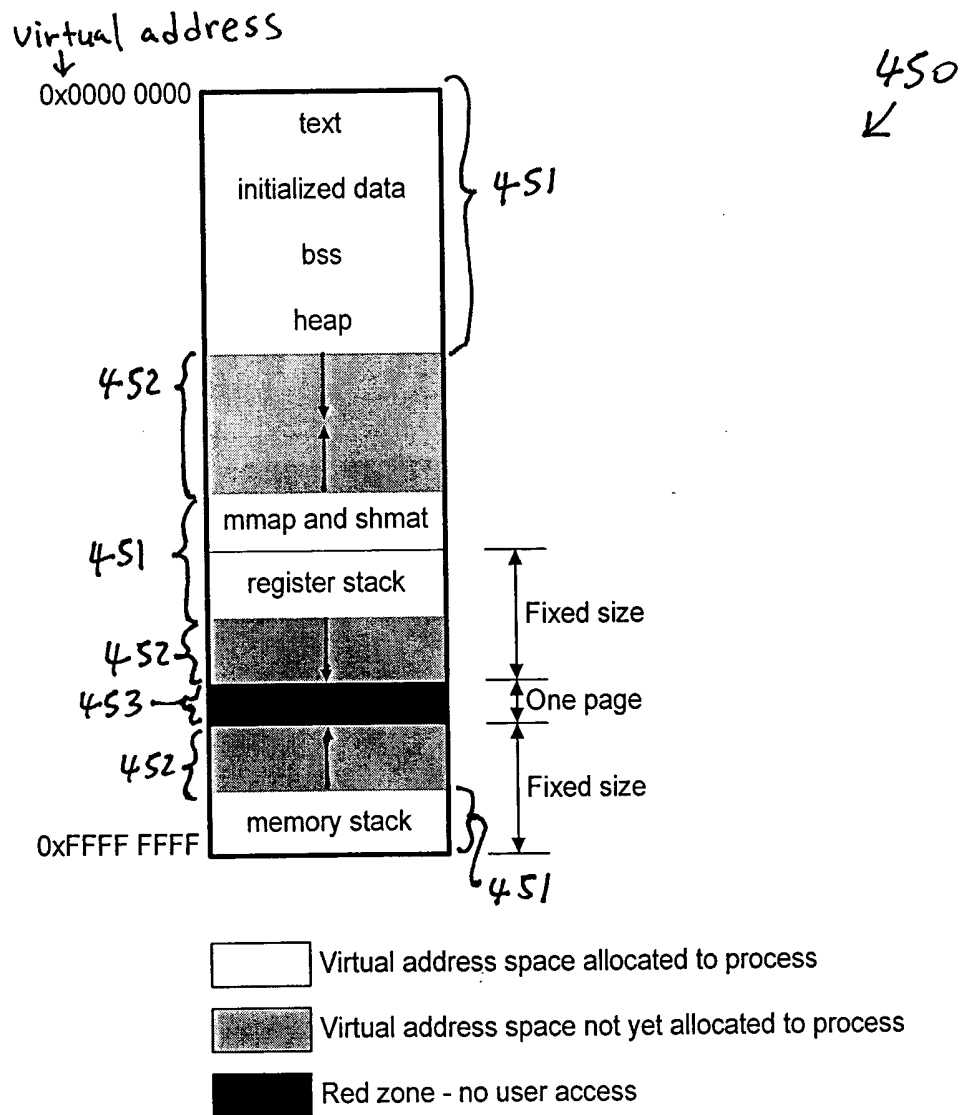


Figure 4B 32bit MPAS in flat representation

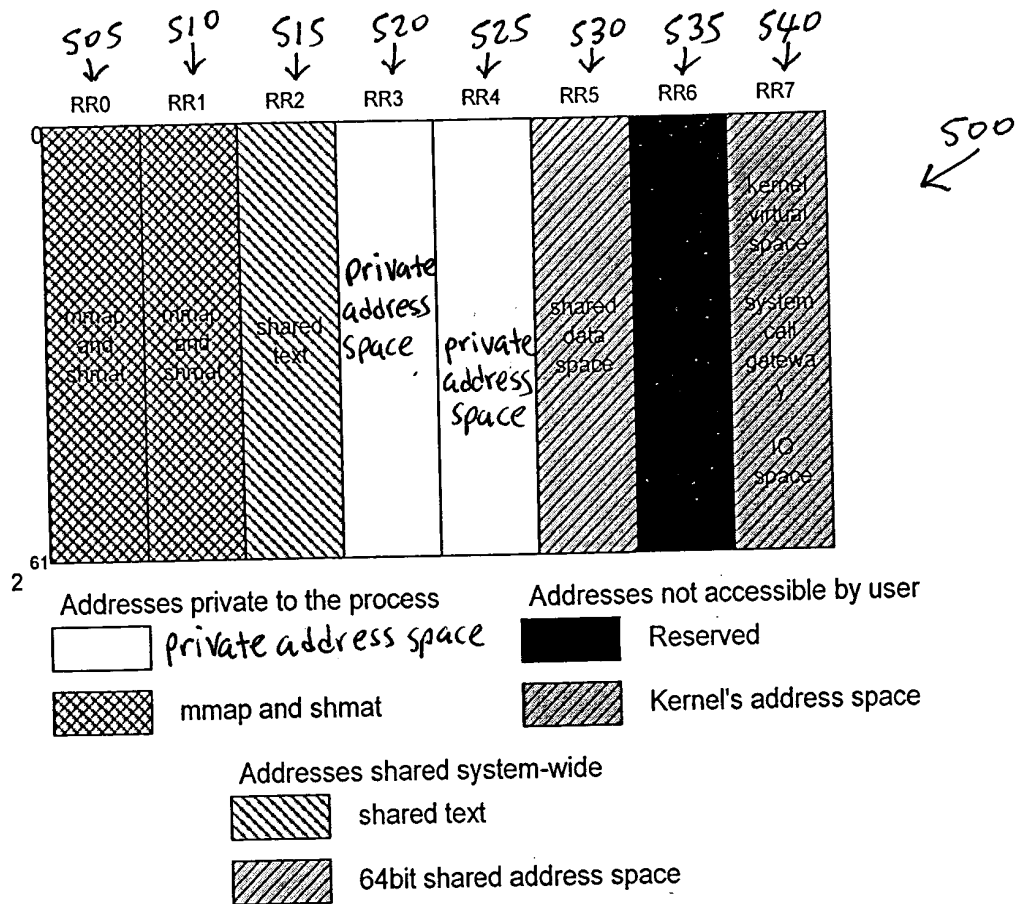


Figure 5A 64 bit MPAS (in segmented representation)

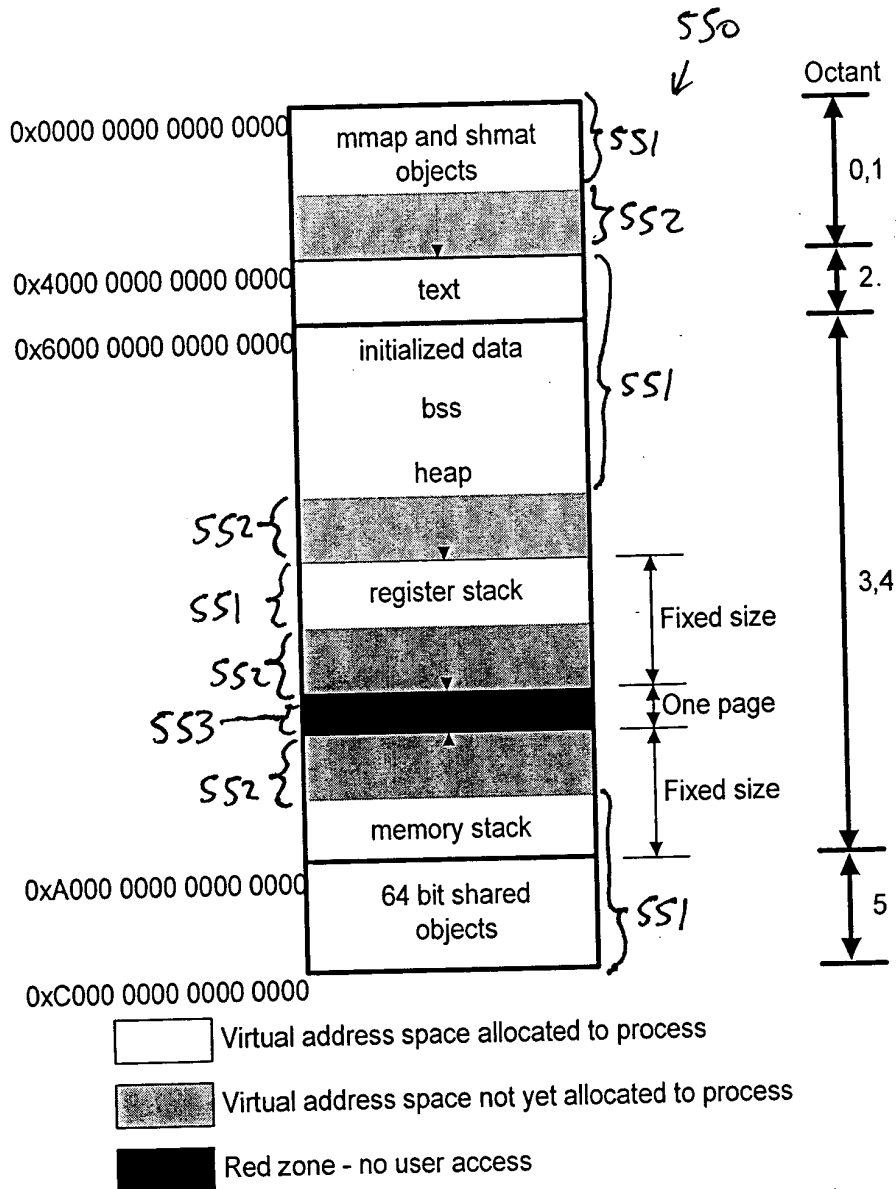


Figure 5B 64 bit MPAS in flat representation (only octants 0-5 are shown)

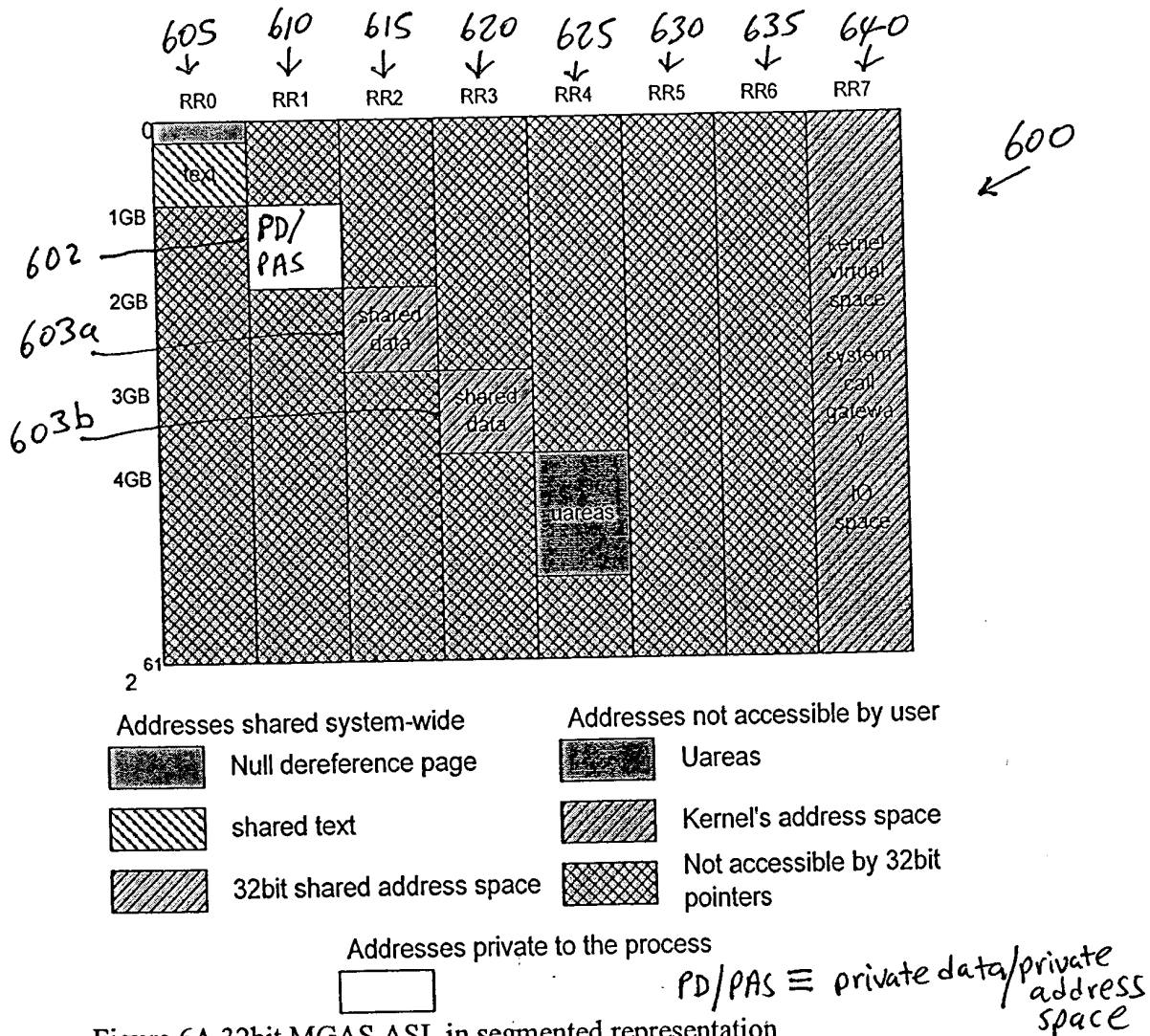


Figure 6A 32bit MGAS ASL in segmented representation

Figure 6A

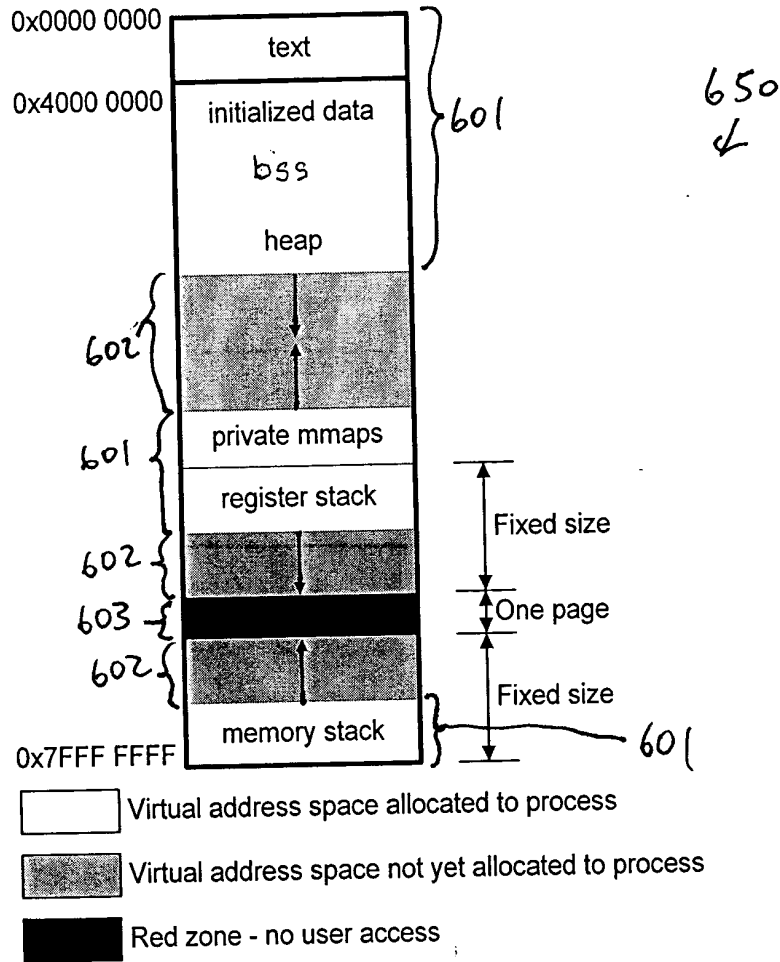


Figure 6B 32bit MGAS ASL in flat representation

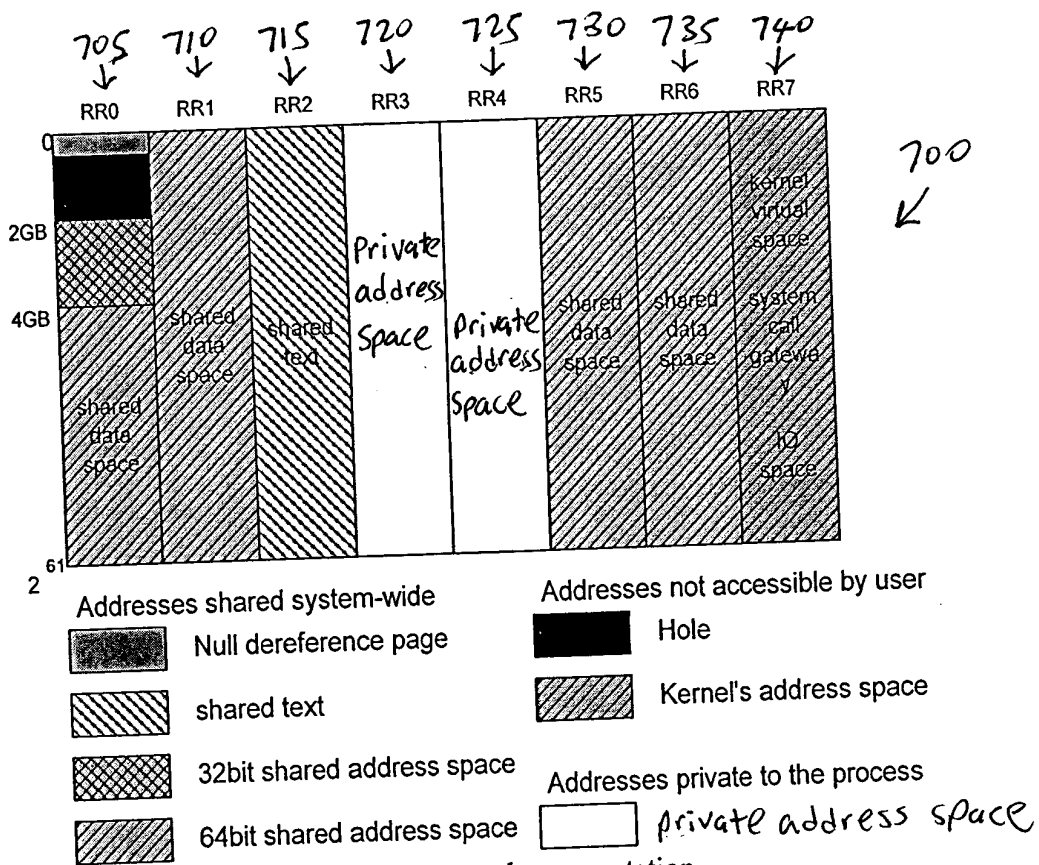
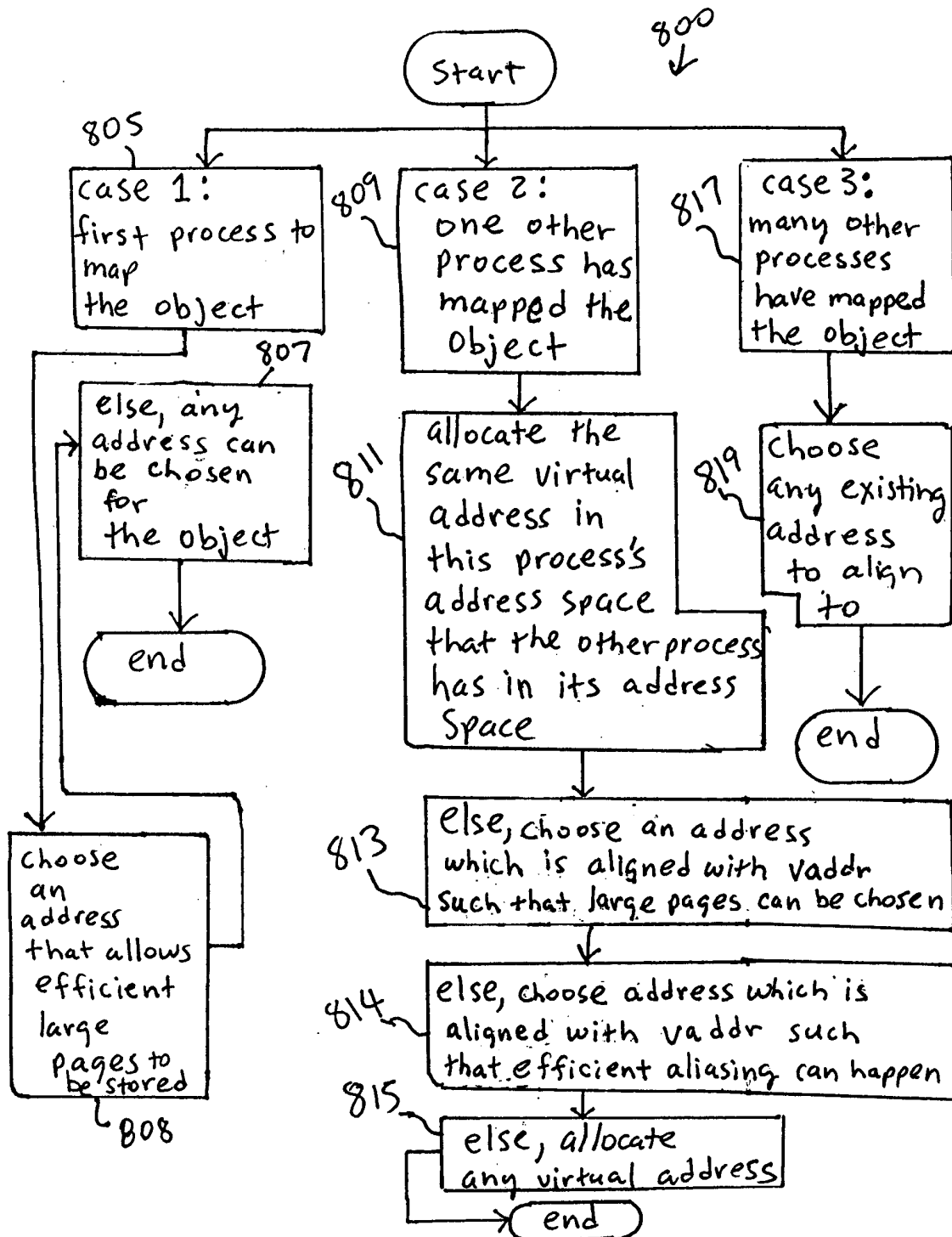


Figure 7 64bit MGAS ASL in segmented representation



Allocating Address Space For 32 bit MPAS Processes
Figure 8

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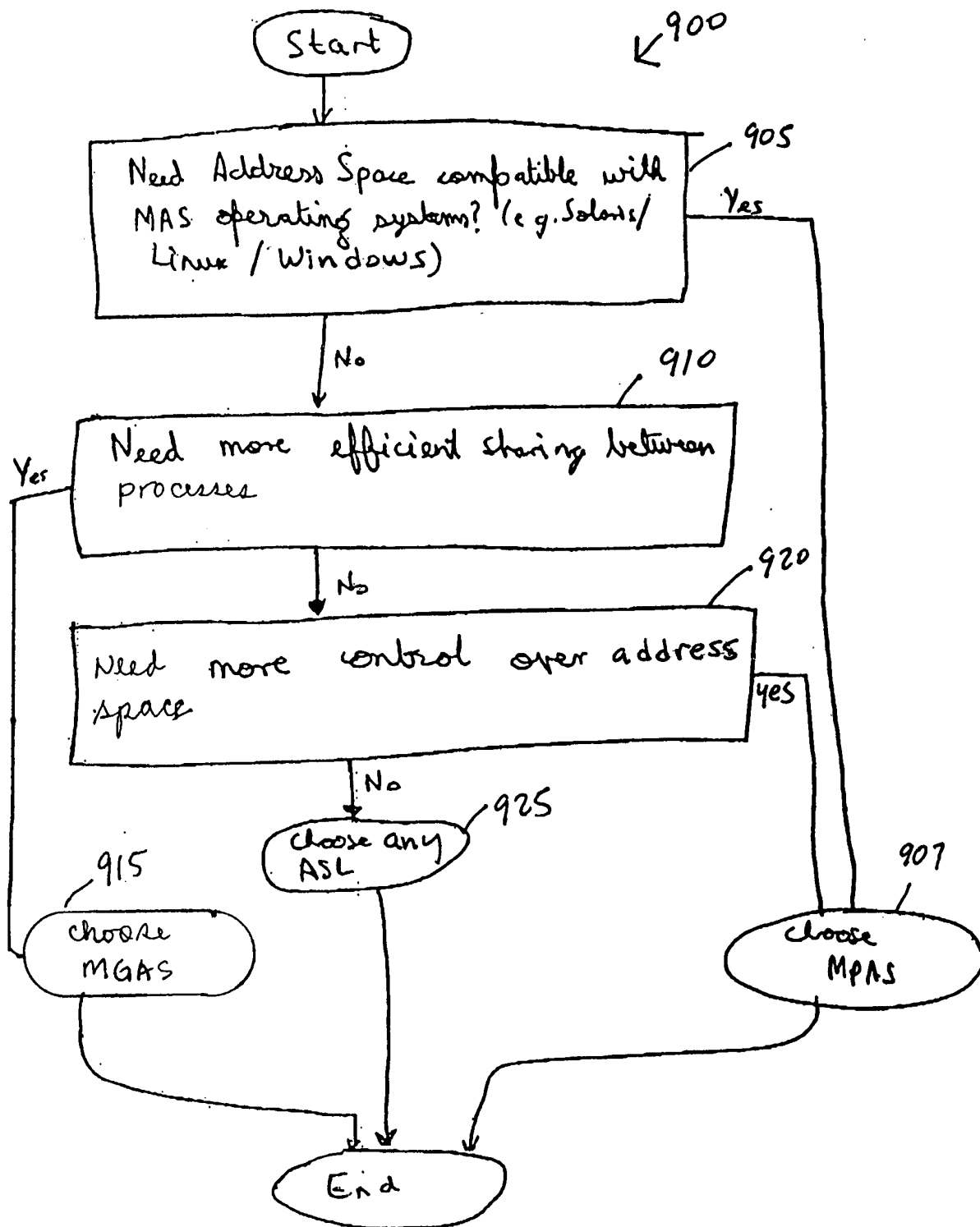


Figure 9

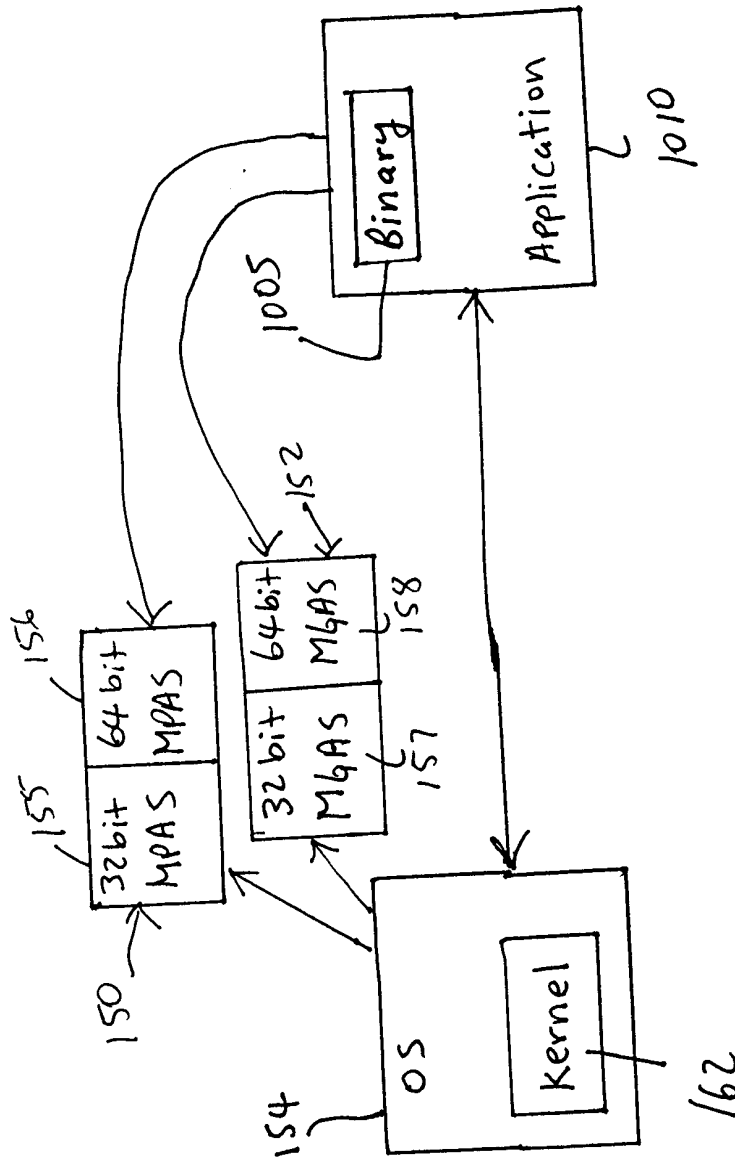


Figure 10